

# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Joshua William CALDWELL and Steven Ashley MARTINEZ

Serial No.: Group Art Unit:

Filed: 10/6/2003 Examiner:

Title: CURRENT LIMITING VOLTAGE REGULATION CIRCUIT

The Commissioner of Patents and Trademarks  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

## Information Disclosure Statement Submitted Pursuant to 37 C.F.R. 1.97(b)

The citations referenced herein, copies attached, may be material to the examination of the above-identified application and are, therefore, submitted in compliance with the duty of disclosure as defined in 37 C.F.R. 1.56. The Examiner is requested to make these citations of official record in the application.

This Information Disclosure Statement submitted in accordance with 37 C.F.R. 1.97(b) is not to be construed as a representation that a search has been made, that additional items material to the examination of this application do not exist, or that any one or more of these citations constitute prior art under 35 U.S.C. 102.

The Examiner's attention is respectfully directed to the following U.S. Patents:


<u>Pat. No.</u>	<u>Pat. Title</u>	<u>Grant Date</u>
6,285,177	SHORT-CIRCUIT CURRENT-LIMIT CIRCUIT	9/4/2001
5,955,915	CIRCUIT FOR LIMITING THE CURRENT IN A POWER TRANSISTOR	9/21/1999
6,426,886	OVERCURRENT PROTECTION FOR A LINEAR POST-REGULATOR USED IN A VOLTAGE CONVERTER SYSTEM	7/30/2002
6,069,950	DUAL-LIMIT CURRENT-LIMITING BATTERY-FEED CIRCUIT FOR A DIGITAL LINE	5/30/2000
5,550,700	INTERCHANGE CIRCUIT OVERLOAD PROTECTION USING DRIVER CURRENT LIMITING	8/27/1996
6,144,187	POWER MEASUREMENT FOR ADAPTIVE BATTERY CHARGER	11/7/2000

Please direct all correspondence concerning the above-identified application to the following address:

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Respectfully submitted,

Date: October 6, 2003

By:   
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
Patent Application

Inventor(s): Joshua William CALDWELL and Steven Ashley MARTINEZ      Group Art Unit:

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**Form 1449**

**U.S. Patent Documents**

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
	A	6,285,177	9/4/01	Mallikarjunaswamy et al.	323	315	5/8/2000
	B	5,955,915	9/21/99	Edwards	327	541	2/13/96
	C	6,426,886	7/30/02	Goder	363	56.1	8/3/01
	D	6,069,950	5/30/00	Knollman	379	413	11/6/97
	E	5,550,700	8/27/96	Moore, et al.	361	101	10/7/94
	F	6,144,187	11/7/00	Bryson	320	137	7/13/99
	G						
	H						
	I						
	J						
	K						

**Foreign Patent or Published Foreign Patent Application**

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
	L							
	M							
	N							
	O							
	P							
	Q							

**Other Documents**

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	R	
	S	
	T	
Examiner		Date Considered

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.  
 Include copy of this form with next communication to applicant.